Unit 1: Introduction to Microprocessor (6 Hrs.)

BIM – 3rd Semester

Prime College

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CONTENTS

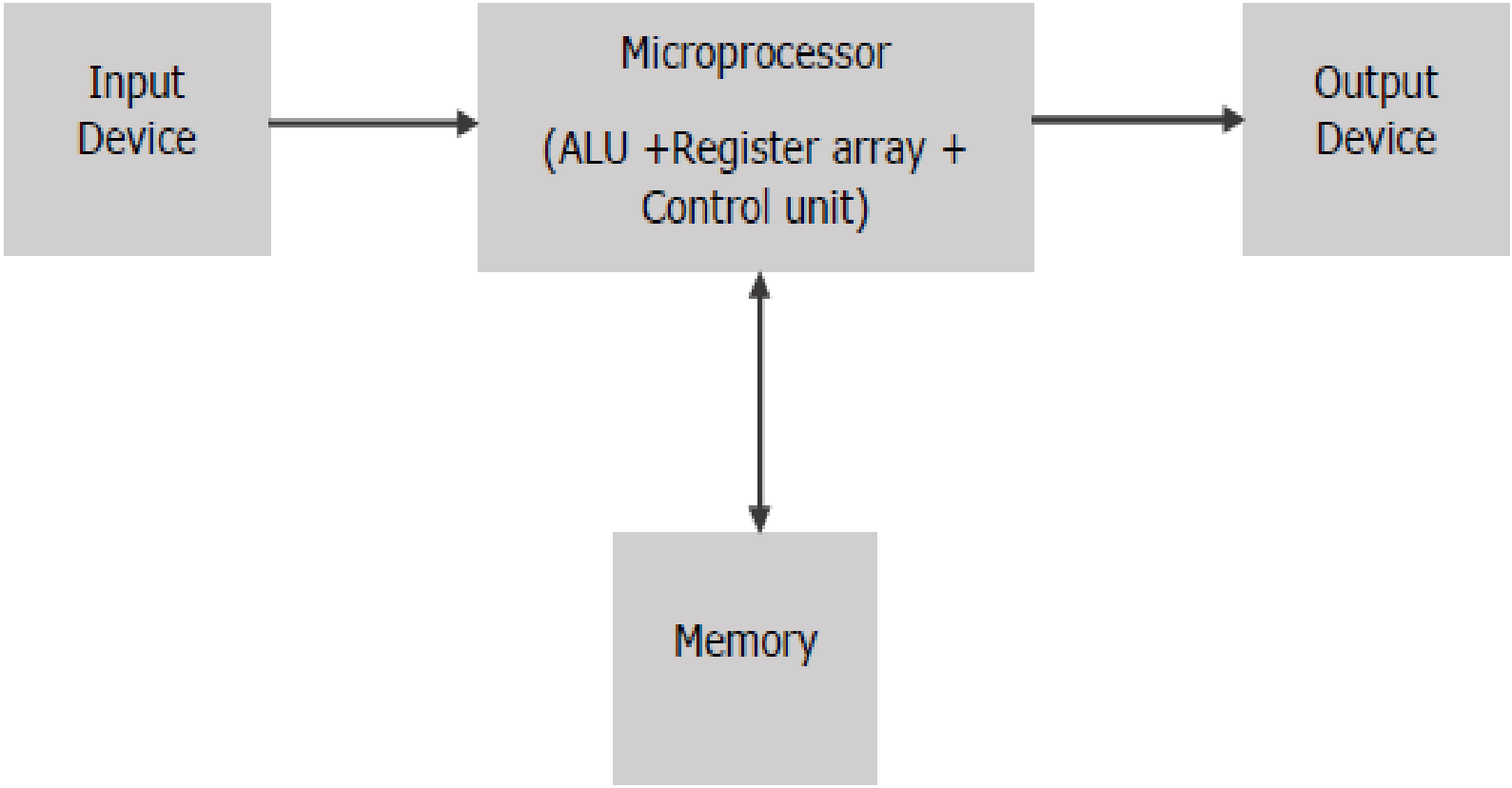
- Microprocessor Components: Registers, ALU, Control and Timing; System Buses; Microprocessor Systems with Bus Organization; Introduction to SAP1 and SAP2

What is Microprocessor?

- Microprocessor is a controlling unit of a micro-computer, fabricated on a small chip capable of performing ALU (Arithmetic Logical Unit) operations and communicating with the other devices connected to it.
- A microprocessor is a multipurpose programmable, clock driven, register based electronic device that reads binary instructions from a storage device called memory, accepts binary data as input, processes data according to those instructions and provide results as output.
- In other words, a microprocessor is a clock driven semiconductor device consisting of electronic circuits.

- Microprocessor is capable of performing various computing functions and making decisions to change the sequence of program execution.
- Microprocessor consists of an ALU, register array, and a control unit. ALU performs arithmetical and logical operations on the data received from the memory or an input device. Register array consists of registers identified by letters like B, C, D, E, H, L and accumulator (register in which intermediate arithmetic and logic results are stored.). The control unit controls the flow of data and instructions within the computer.

Block Diagram of a Basic Microcomputer



Terms Used

CPU: Central processing unit which consists of ALU and control unit.

Microprocessor: Single chip containing all units of CPU.

Microcomputer: Computer having microprocessor as CPU.

Microcontroller: Single chip consisting of MPU, memory, I/O and interfacing circuit.

MPU: Micro processing unit – complete processing unit with the necessary control signals.

How does a Microprocessor Work?

- The microprocessor follows a sequence: Fetch, Decode, and then Execute.
- Initially, the instructions are stored in the memory in a sequential order.
- The microprocessor fetches those instructions from the memory, then decodes it and executes those instructions till STOP instruction is reached.
- Later, it sends the result in binary to the output port.
- Between these processes, the register stores the temporarily data and ALU performs the computing functions.

Features of a Microprocessor

a) Cost-effective − The microprocessor chips are available at low prices and results its low cost.

b) Size − The microprocessor is of small size chip, hence is portable.

c) Low Power Consumption − Microprocessors are manufactured by using metal oxide semiconductor technology, which has low power consumption.

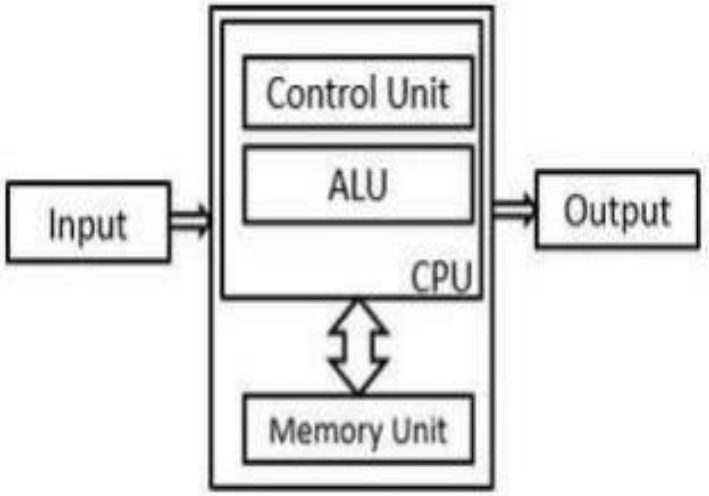
d) Versatility − The microprocessors are versatile as we can use the same chip in a number of applications by configuring the software program.

e) Reliability − The failure rate of microprocessors is very low, hence it is reliable.

Von Neumann Architecture

- Von Neumann architecture was first published by John von Neumann in 1945.
- His computer architecture design consists of a Control Unit, Arithmetic and Logic Unit (ALU), Memory Unit, Registers and Inputs/Outputs.
- Von Neumann architecture is based on the stored-program computer concept, where instruction data and program data are stored in the same memory. This design is still used in most computers produced today.
- The modern computers are based on a stored-program concept introduced by John von Neumann. In this stored-program concept, programs and data are stored in a separate storage unit called memories and are treated the same. Von Neumann architecture requires only one bus for instruction and data

As shown in figure, the main memory is used to store both data and instructions. The ALU is capable of performing arithmetic and logical operations on binary data. The program control unit interprets the instructions in memory and causes them to be executed. The I/O unit gets operated from the control unit.

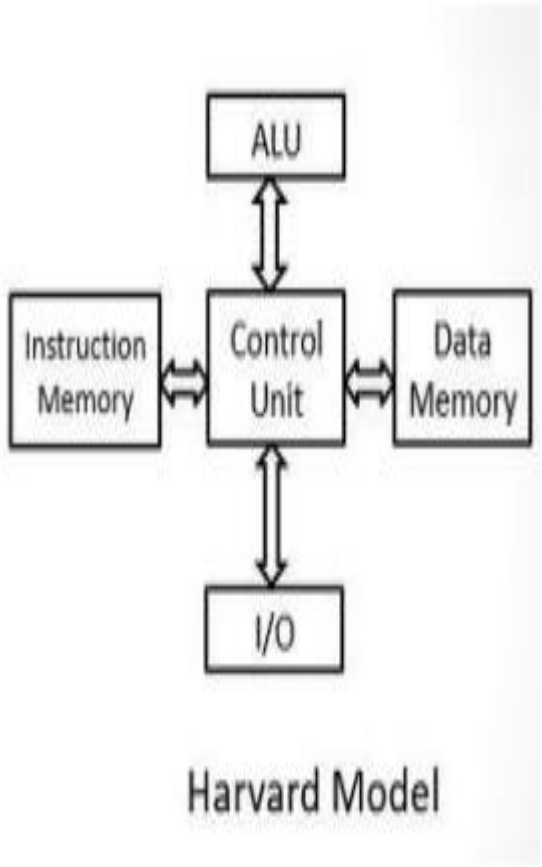


- Main memory is used to store both data and instruction
- ALU is capable for performing Arithmetic and logical operation binary data.
- The program control unit (CPU) interprets the instruction in memory and causes them to be a execute.
- The input/output unit and helps inputting data and getting results. The memory of Von-Neumann machine consists of thousand storage location called words of 40 binary digits(bits).
- Both data and instruction are stored in it. The storage locations of control unit and ALU are called registers. The various registers of this model are MBR, MAR, IR, IBR, PC, AC.

- **Memory Buffer Register (MBR):** It consist of a word to be stored in memory or is used to receives a memory or is used to receive a word from memory.
- **Memory address Register(MAR):** It contain the address in memory of the world to be written from or read into the MBR.
- **IR(Instruction register):** Contain the 8 bit opcode (operation code) instruction being executed. IBR(instruction buffer register): It is used to temporarily hold the instruction from a word in memory.
- **PC (program counter):** It contain address of next instruction to be fetched from memory.
- **AC (Accumulator) and MQ(multiplier quotient):** They are employed to temporarily hold operands and results of ALU operations.

Harvard Architecture

- The Harvard architecture is a computer architecture with physically separate storage and signal pathways for instructions and data. The term originated from the Harvard Mark I, which stored instructions on punched tape and data in electro-mechanical counters.
- These early machines had data storage entirely contained within the central processing unit, and provided no access to the instruction storage as data.
- It required two memories for their instruction and data. Harvard architecture requires separate bus for instruction and data.



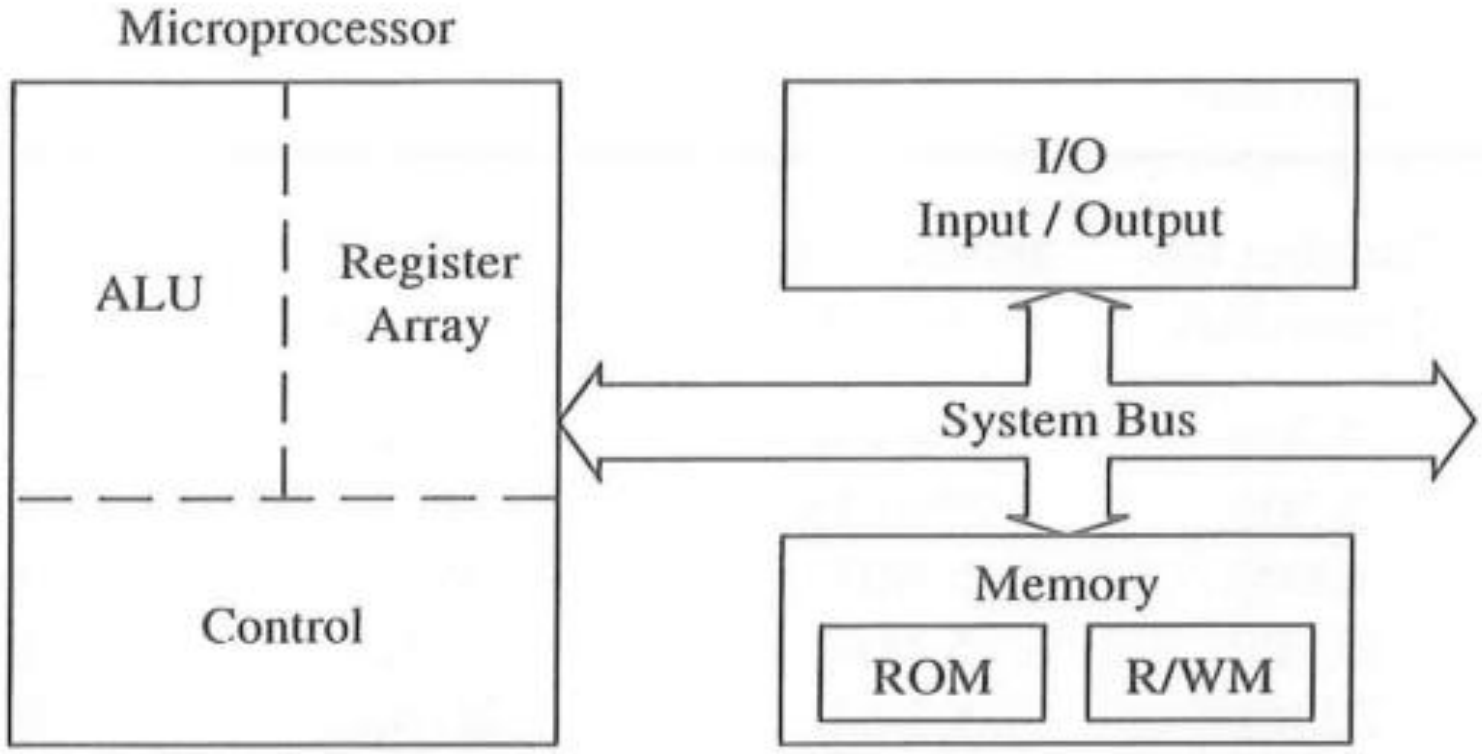
- **Arithmetic and Logic Unit:** The arithmetic logic unit is part of the CPU that operates all the calculations needed. It performs addition, subtraction, comparison, logical Operations, bit Shifting Operations, and various arithmetic operations.
- **Control Unit:** The Control Unit is the part of the CPU that operates all processor control signals. It controls the input and output devices and also controls the movement of instructions and data within the system.
- **Input/Output System:** Input devices are used to read data into main memory with the help of CPU input instruction. The information from a computer as output is given through Output devices. The computer gives the results of computation with the help of output devices.

Von Neumann vs Harvard architecture

	Von Neumann Architecture	Harvard Architecture
Flexibility	High level of flexibility as the memory is shared between instructions and data so the level assigned to each can fluctuate depending on task	Limited flexibility as there is only a certain amount of memory that can be used for data and a certain amount for instructions.
Speed	Speed is limited when compared to harvard due to only having one memory location and set of buses	Two sets of memory and buses mean data can be handled more quickly which would result in decreasing execution time
Examples	Typically used in general purpose computers that will be used for many different purposes.	Typically embedded systems like washing machines, burglar alarms etc.

Note: Burglar alarm: an electronic device that emits a loud noise or other alert when someone attempts to gain unauthorized entry to a building or other premises.

Microprocessor Architecture & Operation



a) Arithmetic /Logic Unit:

ALU performs arithmetic and logical operations on the data received from the memory or an input device. The arithmetic operations like addition and subtraction and logical operations like AND, OR and XOR.

b) Register Array:

The registers are primarily used to store data temporarily during the execution of a program and are accessible to the user through instruction. Register array consists of registers identified by letters like B, C, D, E, H, L, MAR, MBR, PC, IR and accumulator (register in which intermediate arithmetic and logic results are stored.).

c) Control Unit:

It provides the necessary timing and control signals to all the operations in the microcomputer. It controls the flow of data between the microprocessor and memory and peripherals.

d) Input:

The input section transfers data and instructions in binary from the outside world to the microprocessor. It includes such devices as a keyboard, switches, a scanner, and an analog-to-digital converter.

f) Output :

The output section transfers data from the microprocessor to such output devices as LED, CRT, printer, magnetic tape, or another computer.

g) Memory:

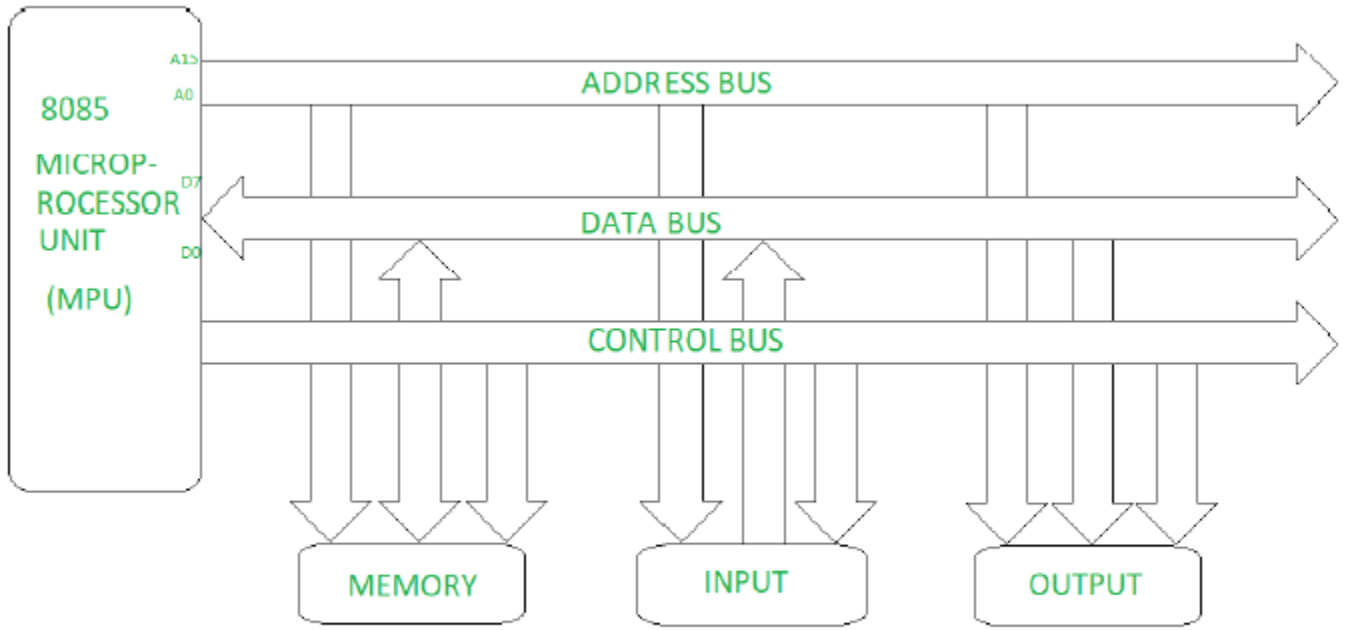
It stores such binary information as instructions and data, and provides that information to the microprocessor. To execute programs, the microprocessor reads instructions and data from memory and performs the computing operations in its ALU section. Results are either transferred to the output section for display or stored in memory for later use.

h) System bus:

It is a communication path between the microprocessor and peripherals. The microprocessor communicates with only one peripheral at a time. The timing is provided by the control unit of the microprocessor.

Bus organization of microprocessor

Bus is a group of conducting wires which carries information, all the peripherals are connected to microprocessor through bus.



Bus organization system of 8085 Microprocessor

There are three types of buses.

a) Address bus :

- It is a group of conducting wires which carries address only.
- Address bus is unidirectional because data flow in one direction, from microprocessor to memory or from microprocessor to Input/output devices.
- Length of address bus of 8085 microprocessor is 16 bit.

b) Data bus :

- It is a group of conducting wires which carries Data only.
- Data bus is bidirectional because data flow in both directions, from microprocessor to memory or Input/output devices and from memory or Input/output devices to microprocessor.
- Length of data bus of 8085 microprocessor is 8 bit.

c) Control bus –

It is a group of wires, which is used to generate timing and control signals to control all the associated peripherals, microprocessor uses control bus to process data, that is what to do with selected memory location. Some control signals are:

- Memory read
- Memory write
- I/O read
- I/O Write

Applications

- The microprocessor is used in personal computers (PCs).
- The microprocessor is used in LASER printers for good speed and making automatic photo copies.
- The microprocessor is used in medical instrument to measure temperature and blood pressure.
- It is used in accounting system and data acquisition system.
- It is used in military applications.
- It is also used in traffic light control.
- Microprocessor is used in home appliances such as microwave ovens, washing machine etc.

Microprocessor Vs Microcontroller

Microprocessor	Microcontroller
CPU is stand alone, RAM,ROM, I/O & timer are separate.	CPU, RAM,ROM, I/O & timer all are on single chip.
Designer can decide amount of RAM,ROM, & I/O ports.	Fixed amount of on-chip RAM,ROM, & I/O ports.
High processing power	Low processing power
High power consumption	Low power consumption
Typically 32/64 bit	8/16 bit
General purpose	Single purpose(control oriented)
Less reliable	Highly reliable
Eg.- 8086,8085	8051

Basic Computer Architecture Design

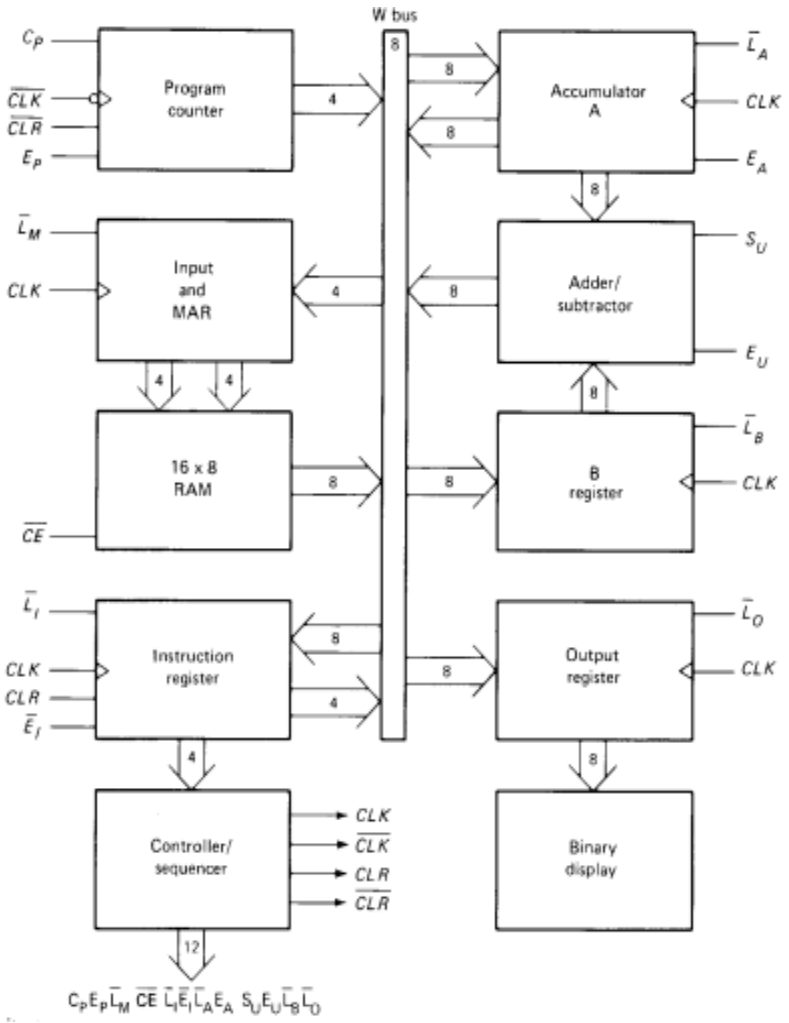
- SAP – I
- SAP – II
- SAP -> Simple as Possible.

SAP – I

- SAP 1 is the first stage in the evolution towards modern computer.
- The main purpose of SAP is to introduce all the crucial ideas behind computer operations.
- Being a simple computer SAP-1 also covers many advance concepts.
- SAP-1 is a bus organized computer. All registers are connected to the W bus with the help of tri-state buffers.

SAP-1 Computer Architecture

- The SAP-1 computer is a bus-organized computer and makes use of Von-Neumann architecture. It makes use of an 8-bit central bus and has ten main components. A pictorial representation of its architecture is shown below. Each of the individual components that make up this computer are described right after.



- All register outputs to the W bus are three state; this allows orderly transfer of data.
- All other register outputs are two state; these outputs continuously drive the boxes they are connected to.

SAP-1 Components

Program Counter: The program counter's job is to store and send out the memory address of the next instruction to be fetched and executed. The program counter, which is part of the control unit, counts from 0000 to 1111 as the program is stored at the beginning of the memory with the first instruction at binary address 0000, the second instruction at address 0001, the third at address 0010, and so on. At the start of each computer run, the program counter is reset to 0000. When the computer run starts, the program counter sends out the address 0000 to the memory and is then incremented by 1. After the first instruction is fetched and executed, the program counter sends the next address 0001 to the memory and again, after that, the program counter is incremented. In this way, the program counter keeps track of the next instruction to be fetched and executed.

Input and Memory Address Register (MAR): The MAR stores the 4-bit address of data or instruction which are placed in memory. When the SAP-1 is running, the 4-bit address is gotten from the Program Counter through the W-bus and then stored. This stored address is sent to the RAM where data or instructions are read from.

Random-Access Memory (RAM): The SAP-1 makes use of a 16 x 8 RAM (16 memory locations each storing 8 bits of data). The RAM can be programmed by means of the address and data switches allowing you to write to the memory before a computer run. During a computer run, the RAM receives its 4-bit address from the MAR and read operation is performed. In this way the instruction or data word stored in the RAM is placed on the W bus for use in some other part of the computer.

Instruction Register:

- The instruction register is part of the control unit.
- To fetch an instruction from the memory the computer does a memory read operation. This places the contents of the addressed memory location on the W-bus.
- At the same time, the IR is set up for loading on the next positive clock edge.
- The contents of the IR are split into two nibbles.
- The upper nibble is a two state output that goes directly to the block labeled 'Controller-sequencer’.
- The lower nibble is a three state output that is read onto the W-bus when needed.

Controller-Sequencer

- Before each computer run, (CLR)' signal is sent to the PC and CLR signal to the IR.
- This resets the PC to 0000 and wipes out the last instruction in the IR
- A clock signal CLK is sent to all buffer registers, this synchronizes the operation of the computer.
- The 12 bits that come out of the CS form a word controlling the rest of the computer The 12 wires carrying the control word are called the control bus.
- The control word has the format:

$$\mathbf{CON} = C_P E_P \overline{L}_M \overline{CE} \quad \overline{L}_I \overline{E}_I \overline{L}_A E_A \quad S_U E_U \overline{L}_B \overline{L}_O$$

- This word determines how the registers will react to the next positive CLK edge.

- For instance, a high Ep and a low Lm’ means that the contents of the program counter are latched into the MAR, on the next positive clock edge. As another example, a low CE’ and a low La’, mean that the addressed RAM word will be transferred to the accumulator on the next positive clock edge.

Accumulator: The accumulator is an 8-bit buffer register that stores intermediate answers during a computer run. The accumulator has two outputs. The two-state output goes directly to the adder-subtractor and the three-state output goes to the bus. This implies that the 8-bit accumulator word continuously drives the adder- subtractor but only appears on the W bus when Ea is high.

Adder-Subtractor: The adder-subtractor asynchronously adds to or subtracts a value from the accumulator depending on the value of Su. It makes use of 2's complement to achieve this

When Su is low the output of the adder-subtractor is the sum of the values in the accumulator and in the B-register (O/P = A + B).

When Su is high, the output is the difference between them (O/P = A + B'+1).

B-Register: The B-register is a buffer register used in performing arithmetic operations. It supplies the number to be added or subtracted from the contents of the accumulator to the adder/subtractor. When data is available at the bus and Lb' is low, at the positive clock edge, B register gets and stores the data.

Output Register: The output register gets and stores the value stored in the accumulator usually after the performance of an arithmetic operation. The answer that is stored in the accumulator is loaded into the output register through the W bus. This is done in the next positive clock edge when Ea is high and Lo is low. The processed data can now be displayed to the outside world.

Binary Display: The binary display is row of eight light emitting diodes(LEDs). The binary display shows us the contents of the output by connecting each LED to the output of the output register. This therefore enables viewing of the answer transferred from the accumulator to the output register in binary.

Instructions of SAP 1

Mnemonic	Operation	OPCODE
LDA	Load addressed memory contents into accumulator	0000
ADD	Add addressed memory contents to accumulator	0001
SUB	Subtract addressed memory contents from accumulator	0010
OUT	Load accumulator data into output register	1110
HLT	Stop processing	1111

Machine Cycle and Instruction Cycle – SAP1

- SAP1 has six T-states (three fetch and three execute cycles) reserved for each instruction. Not all instructions require all the six T-states for execution. The unused T- state is marked as No Operation (NOP) cycle.
- Each T-state is called a machine cycle for SAP1. A ring counter is used to generate a T-state at every falling edge of clock pulse. The ring counter output is reset after the 6th T-state.
- FETCH CYCLE – T1, T2, T3 machine cycle
- EXECUTE CYCLE - T4, T5, T6 machine cycle

Machine Cycle and Instruction Cycle – SAP1

- Fetch cycle is generally same for all instructions
- Complete code includes opcode and operand
- Like LDA 04H ➔ 0000 0100
- One instruction is executed in one instruction cycle

Fetch Cycle SAP 1

- **Fetch Cycle**
  - Address state: enable PC to bus three-state output, MAR load line
  - Increment state: enable PC increment (and perhaps wait for memory access time)
  - Memory state: enable memory CE, IR load line
- IR is loaded on the low-to-high clock transition, so stabilizes before state 4 is entered
  - t1: MAR ← PC
  - t2: PC ← PC +1
  - t3: IR ← RAM

Execution Cycle SAP 1

- **Execution Cycle – LDA address**
  - t4: MAR ← (IR (Address of operand)) [memory address is sent from IR to MAR]
  - t5: Accumulator ← RAM [data from memory is fetched and sent to AC]
  - t6: nothing (NOP) [do nothing]
- **Execution Cycle – ADD B**
  - t4: MAR ← (IR (Address of B))
  - t5: B ← RAM
  - t6: Accumulator ← Accumulator + B

Diagram of Fetch Cycle

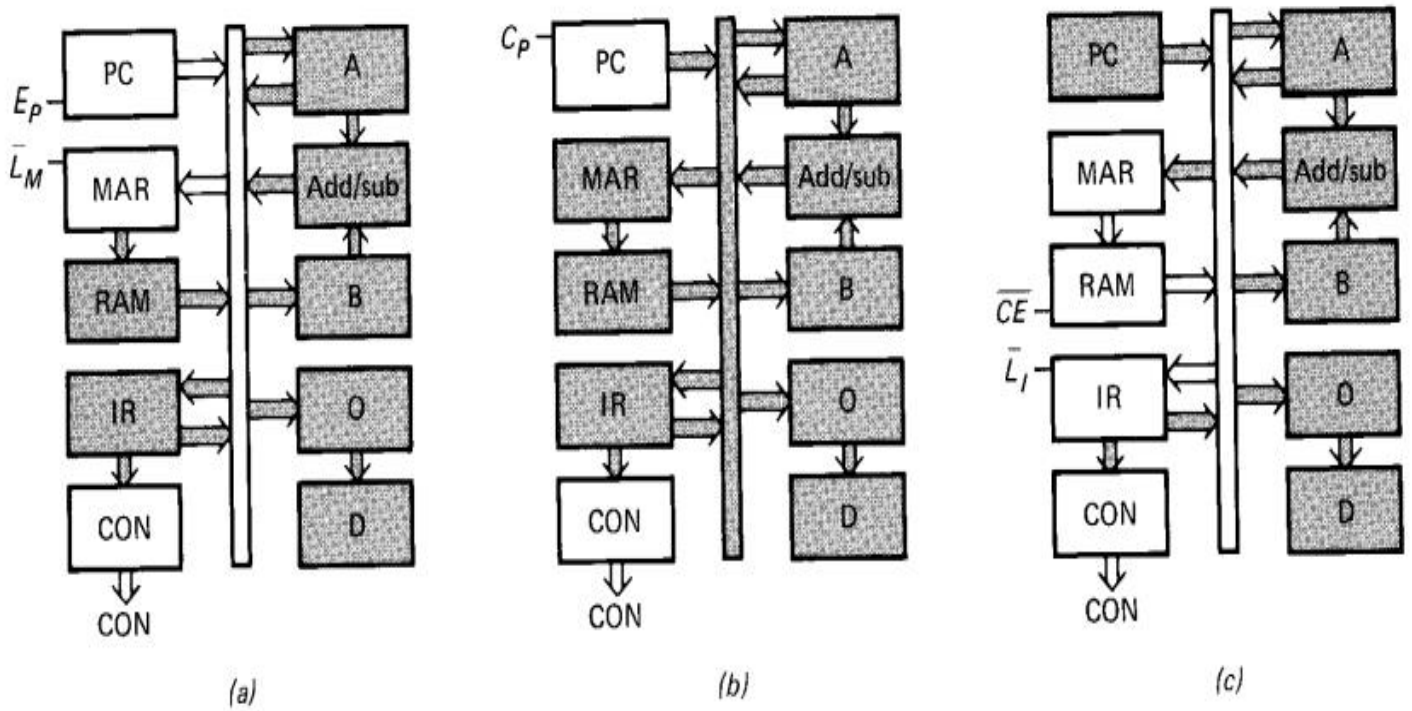


Fig. 10-3 Fetch cycle: (*a*) T_1 state; (*b*) T_2 state; (*c*) T_3 state.

Execution Cycle of LDA

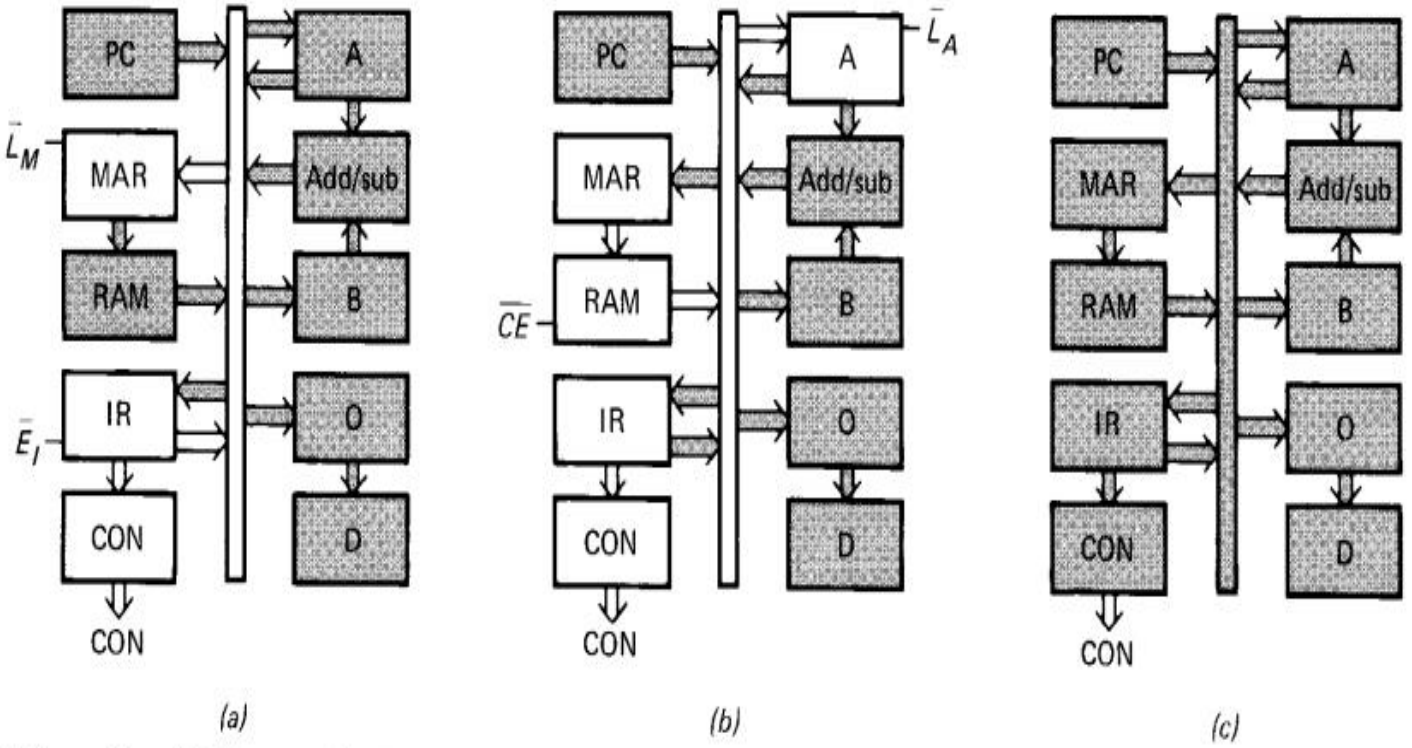
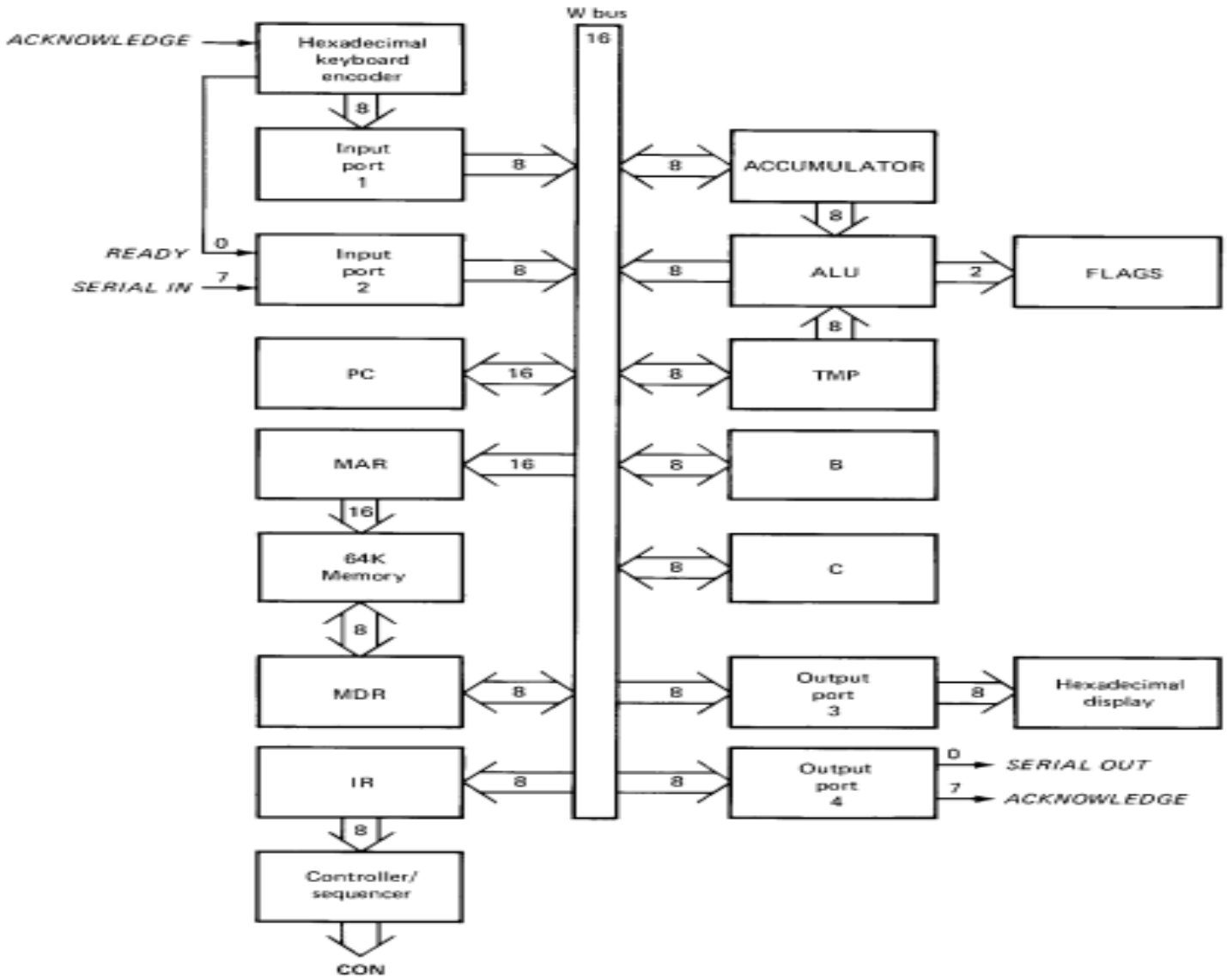


Fig. 10-4 LDA routine: (*a*) T_4 state; (*b*) T_5 state; (*c*) T_6 state.

SAP 2

- Bidirectional registers
- Includes jump instructions
- All register outputs to W bus are three-state; those not connected to the bus are two-state

SAP 2 Block Diagram



SAP 2 Components

- **Input Ports:** SAP-2 has 2 input/output ports: port 1 and port 2. A hexadecimal keyboard encoder is connected to port 1. It allows us to enter hexadecimal instructions and data through port 1. The hexadecimal keyboard encoder sends a ready signal to bit 0 of port 2. This signal indicates when the data in port 1 is valid. SERIAL input can be taken from pin 7 of port 2.
- **Program Counter (PC):** Program Counter can store 16-bit address, therefore it can count from:

  PC-0000 0000 0000 0000 to PC = 1111 1111 1111 1111.

  This equivalent to 0000H to FFFFH (or decimal 0 to 65535).

  The low (CLR)' signal resets the PC before each computer run, so the data processing starts with the instruction stored in memory location 0000H.

- **MAR and Memory**: During the fetch cycle, the MAR receives 16 bit addresses from PC. The two state MAR output then addressed memory location. The memory has 2K ROM with address 0000H too 07FFH.

The ROM contains a program called monitor that initializes the computer on power- up, interprets the keyboard inputs and so on. The rest of memory is 64 K RAM (62 Kb RAM and 2 Kb ROM) with addresses from 0800H to FFFFH.

- **Memory Data Register (MDR):** The MDR is an 8-bit buffer register to store 8-bit Op-code, An 8-bit Op-code can accommodate 256 instructions. SAP-2 has only 42 instructions are identical with 8080/8085 instructions. Its output sets up the RAM. The MDR receives the data from the W-BUS before a write operation and it sends data to the BUS after a read operation.

- **Instruction Register (IR):** SAP-2 has more instructions than SAP-1. Therefore. SAP-2 uses 8 bits for the Opcode rather than 4 bits. An 8 bit Opcode can accommodate 256 instructions, but SAP-2 has only 42 instructions. [Note: All SAP instructions are identical with 8085 instructions]
- **Controller-Sequencer:** The controller-sequencer produces the control word or micro-instructions that coordinates and direct the rest of the computer. Since, SAP-2 has bigger instruction set; the controller-sequencer has more hardware. The control word (CON) or micro-instructions determine how the registers react to the next positive edge dock.

- **Accumulator**: The two-state output of the accumulator goes to the ALU and the three-state output to the W-bus. Therefore, the 8-bit word in the accumulator continuously drives the ALU, but this same word appears on the bus when Ex is active.
- **ALU and Flags:** The ALUS are commercially available as integrated circuit (IC). These ALUS have 4 or more control bits that determine arithmetic and logic operation performed on word A and B. The ALU used in SAP-2 includes arithmetic and logic operation. Flag is a flip-flop that keeps track of a changing condition during computer run. The SAP- 2 has two flags:

Sign Flag: The sign flag is set when the accumulator contents become negative during the execution of some instructions.

Zero Flag: The zero flag is set when the accumulator contents are zero.

- **TMP, B & C Register:** Instead of using B register to hold the data being added to or subtracted from the accumulator a temporary (TMP) register is used. This allows us more freedom in using the B register. Besides these TMP and B registers SAP-2 includes a C register which gives us more computer flexibility in moving data during a computer run.

- **Output Ports:** SAP-2 has two output ports: port 3 and port 4. The contents of the accumulator can be loaded into port 3, which drives the hexadecimal display. This allows us to see the processed data. The contents of the accumulator can also be sent to port 4.

The pin 7 of port 4 sends ACKNOWLEDGE signal to the hexadecimal encoder. This ACKNOWLEDGE signal and READY signal are part of a concept called handshaking. The SERIAL OUT signal from pin 0 of port 4 converts parallel data in the accumulator into serial output data.

SAP-1	Sap-2
It has 8-bit bus.	It has 16-bit bus.
PC is 4-bit.	PC is 16-bit.
It does not have hexadecimal keyboard encoder.	It has hexadecimal keyboard encoder.
It has single input.	It has two input ports.
MAR receives 4-bit address from PC.	MAR receives 16-bit address from PC.
It does not have ROM.	It has 2 KB ROM.
It has 16 KB memory.	It has 62 KB memory.
It does not have MDR.	It has MDR.
It has only adder/subtractor.	It has ALU.
It does not have flag.	It has 2 flags.
It does not have temporary register.	It has temporary register.
It has single register (B).	It has 2 registers (B and C).
It has single output port.	It has 2 output ports.
It has 5 instruction sets.	It has 42 instruction sets.

SAP 2 Instruction Set

LDA	Load to Accumulator	Load accumulator from memory.
STA	Store the Accumulator	Store the accumulator content in memory.
MVI	Move immediate	Move immediate value to register.
MOV	Move	Move from register to register.
ADD	Add	Add register content to A and store in A.
SUB	Subtract	Subtract register content from A and store in A.
INR	Increase Register	
DCR	Decrease Register	
JMP	Jump	
JM	Jump if minus	
JZ	Jump if zero	
JNZ	Jump if not zero	
CALL	Call the subroutine	Call subroutine from given memory location.
RET	Return from subroutine.	

SAP 2 Instruction Set

CMA	Complement the Accumulator	
ANA	And the accumulator	AND accumulator with another register.
ORA	OR thr accumulator	OR accumulator with another register.
ANI	AND immediate	AND with a 8 bit data.
ORI	OR immediate	OR with 8 bit data.
XRI	XOR immediate	XOR with 8 bit data.
NOP	No Operation	
HLT	Halt	Stall the CPU.
RAL	Rotate Accumulator left	
RAR	Rotate Accumulator Right	
IN	Input from port	
OUT	Output to port	