Only for 2021 - 2023 AD admitted Students

TRIBHUVAN UNIVERSITY
FACULTY OF MANAGEMENT
Office of the Dean
November 2024

Full Marks: 60
Pass Marks: 30
Time: 3 Hrs.

BIM / Second Semester / IT 233: Digital Logic

Candidates are required to answer the questions in their own words as far as practicable

Group "A"

Brief Answer Questions: ***[10×1=10]***

1. What is BCD Code?
2. Define Decoder.
3. Mention any two differences between combinational and sequential circuit.
4. What is triggering of a Flip-flop?
5. Define counter.
6. What is the use of k-map?
7. Convert $(1010)_2$ to gray code.
8. What is shift Register?
9. Define canonical form.
10. What is clock pulse?

Group "B"

Short Answer Questions: (Attempt any FIVE Questions) ***[5×3=15]***

11. Convert $(101011.1101)_2$ to Octal and Hexadecimal form.
12. Realize the property of NOR gate and NOT gate using NAND gate.
13. Find the value of $(279)_{10} + (799)_{10}$ by converting it to BCD data.
14. Design half adder using NAND gates.
15. Illustrate and explain basic Flip-Flop.
16. Design a 3-bit Asynchronous counter.

Group "C"

Long Answer Questions: (Attempt any THREE Questions) ***[3×5=15]***

17. Illustrate and explain JK Flip-Flop.
18. Design 1 × 4 De-multiplexer.
19. Design MOD-7 synchronous counter.
20. Minimize the following Boolean function: $f(P,R,S,Q) = \sum(0,2,3,7,8,10,13,15)$ and draw circuit diagram using only NOR gates.

Group "D"

Comprehensive Answer / Case / Situation Analysis Questions: ***[2×10=20]***

21. Design a four bit parallel In/shift right/serial out shift register. Also illustrate how binary data$(1011)_2$ is load and retrieved in your design circuit.

22. If the content of Register A is $(1011)_2$ and Register B is $(1101)_2$. Design a combinational circuit for adding the content of these two register.