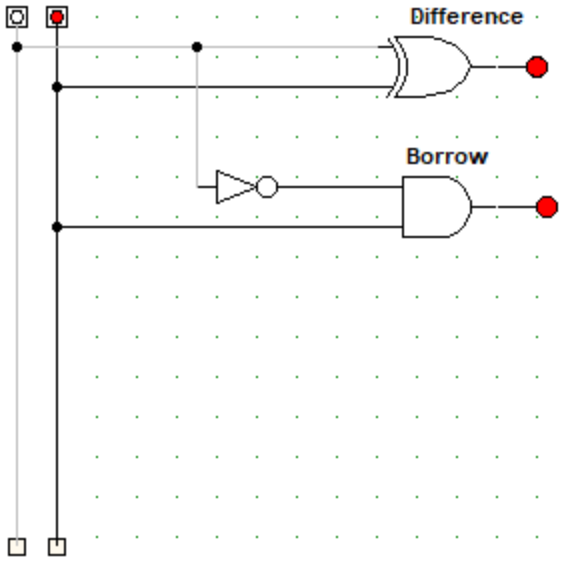
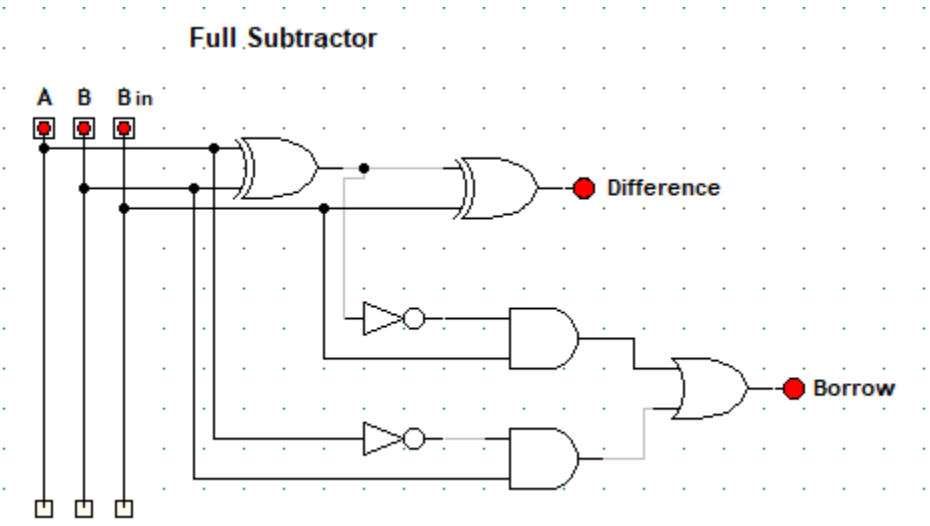
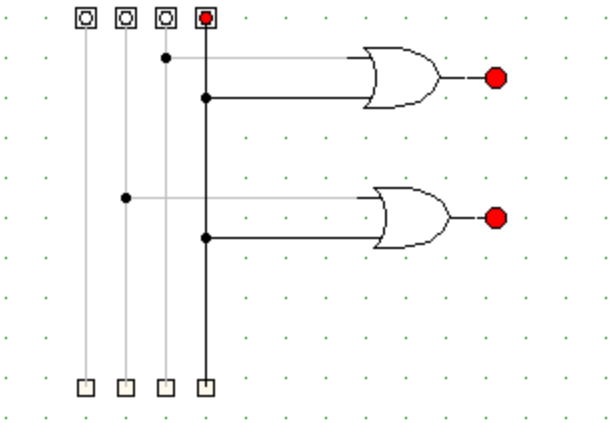
Half Subtractor



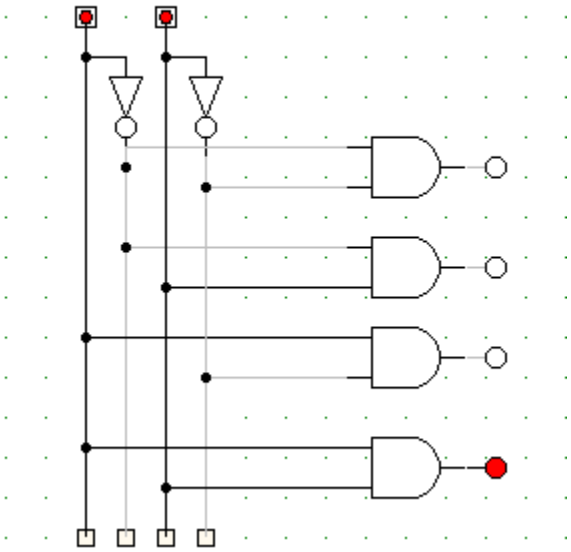
Full Subtractor



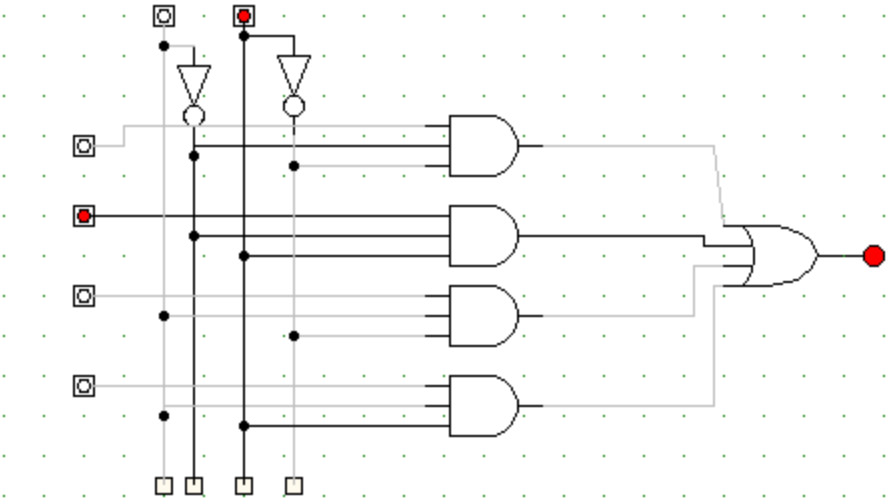
Experiment Diagram of 4*2 Encoder



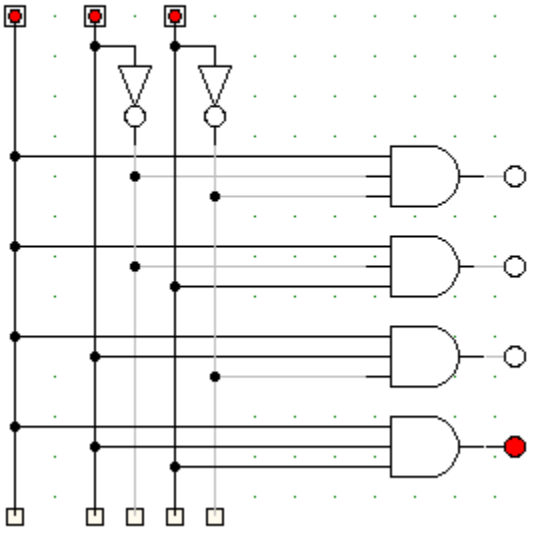
Experiment Diagram of 2*4 Decoder



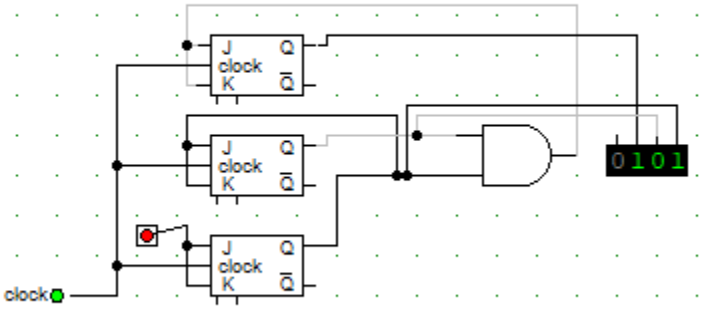
Experiment of 4*1 MUX



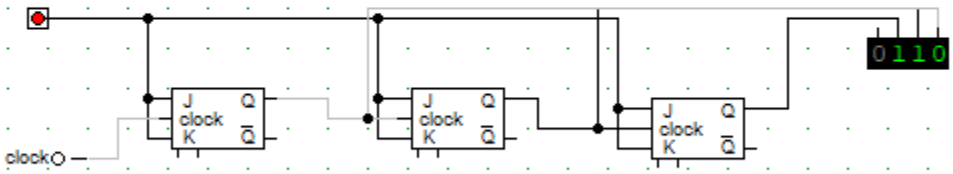
Experiment of 1*4 De-Mux



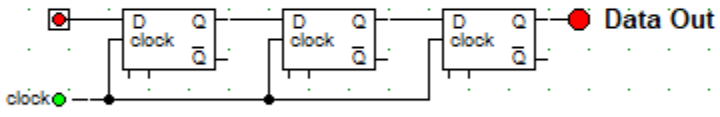
Experiment of 3 bit (mod 8) synchronous up counter



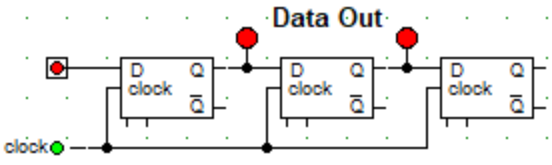
Experiment of 3 bit (mod 8) asynchronous up counter



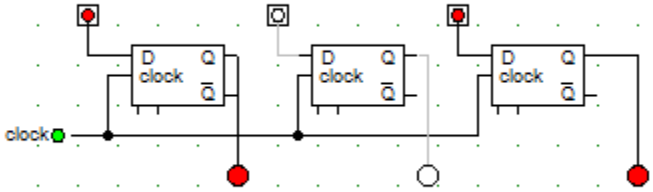
Experiment of 3 bit SISO shift register



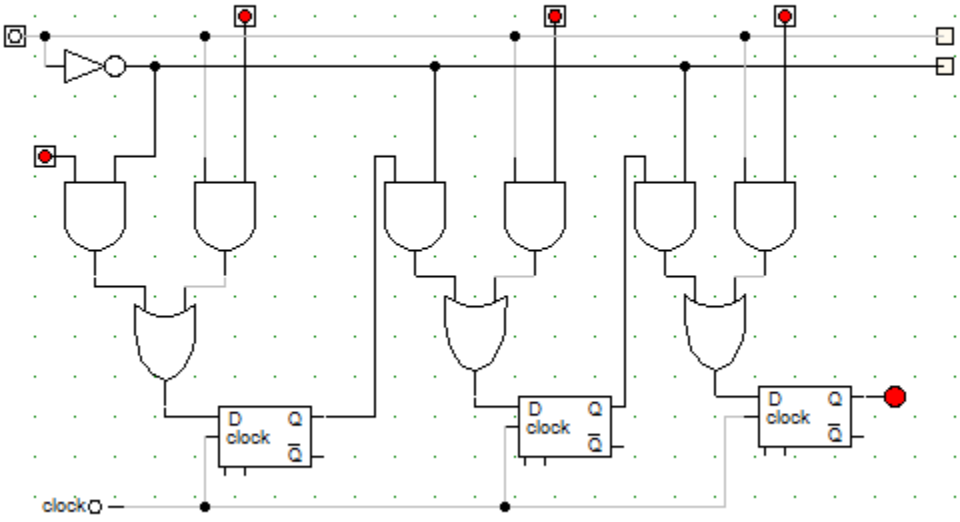
Experiment of 3 bit SIPO shift register

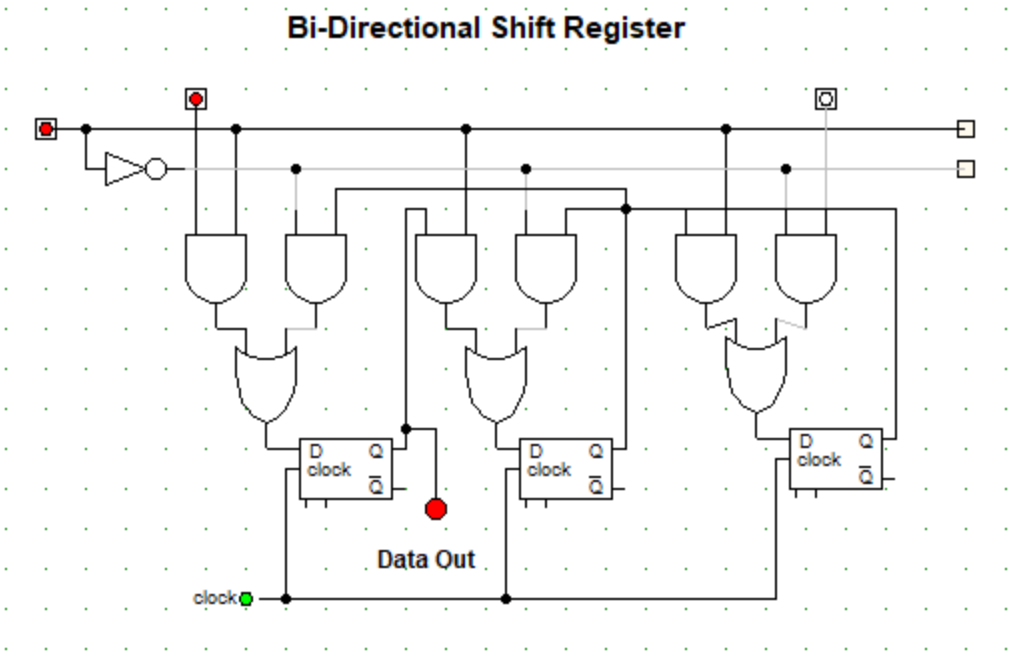


Experiment of 3 bit PIPO shift register



Experiment of 3 bit PISO shift register




Bi-Directional Shift Register
D
clock
Q
Q̄
D
clock
Q
Q̄
D
clock
Q
Q̄
Data Out
clock